

The Examiner states that the drawings are objected to because FIG. 6 shows transistor 602 as an nMOS field effect transistor instead of a p MOS field effect transistor as described in page 30, line 21 and claimed in claim 32. As mentioned above, Applicants have amended FIGS. 6 and 8 to properly show third power switch transistor 602 as a p-MOS power switch transistor, as recited on page 30, last paragraph of the specification.

IV. Status of the Specification

The specification has been amended (paragraph beginning on page 24, line 8) to correct a typographical error. Specifically, the power switch subcircuit was incorrectly referenced as 301 and has been corrected to properly reference 303 as throughout the specification.

V. Claim Rejections under 35 U.S.C. § 112

Claims 26, 31-32, 37, 41 and 43-50 stand rejected under 35 U.S.C. § 112, second paragraph.

Regarding claim 26, the Examiner states that the recitation of “the first power switch transistor is a common power switch transistor provided for the flip flop and for at least one additional flip flop” is indefinite because it is misdescriptive of the present invention. Specifically, the Examiner states that power switch transistor 303 (see figure 3) couples only the additional flip flop (309, 310, 315, 316) to Vss, however flip flop 301 is coupled directly to VDDL and VSS. Therefore, the Examiner states the first power switch transistor is not a common power switch transistor to the flip flop and the additional flip flop.

Applicants respectfully traverse the above rejection. Applicants direct the Examiner to page 10, lines 5-10 of the specification which recites “*a common power switch transistor may be provided for the flip-flop of the circuit arrangement and at least one additional flip-flop. In other words, the power switch transistor according to the invention may be formed jointly for a plurality of flip-flops, thereby reducing the area requirement of the circuit arrangement*”. Also, “*although only a single flip-flop subcircuit 301 is shown in Figure 3, the power switch subcircuit 301 may be shared by a plurality of flip-flop subcircuits 301 and/or by a plurality of pulse generator subcircuits 302.*” See, specification, page 24, lines 11-13. Applicants have added drawing figure 12 illustrating the above feature in block diagram form. No new matter has been added and support for figure 12 can be found on page 10, lines 5-10 and page 24, lines 11-13 of the specification (recited above).

Regarding the Examiner's reference to a flip flop consisting of transistors 309, 310, 315 and 316, Applicants respectfully point out that the transistors 309, 310, 315 and 316 do not function as a flip-flop circuit due to the fact that the clock input 305 controls the transistors 307 and 308 such that when the clock signal CLK goes low, the PMOS transistors 307 and 308 are turned on, thereby putting the node signal /S and /R, respectively, to the VDDL potential. Thus, there is no permanent non-volatile storage of data provided by the four transistors 309, 310, 315 and 316. As discussed in more detail in the specification, these transistors serve for stabilization of the signal and thus function as a pulse generator circuit for generating the flip-flop input signal.

Regarding claims 31, 37, 41, 43-45, 47 and 48 Applicants have amended the claims for correct antecedent basis.

VI. Rejections Under 35 U.S.C. § 102(b)

Claims 24-25 and 27-28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,583,457 to Horiguchi et al. (hereinafter “Horiguchi”).

Regarding claims 24-25 and 27-28, the Examiner states that Horiguchi discloses a circuit arrangement (See Figure 29) comprising a flip flop (LH) having a plurality of storage transistors with a threshold voltage of a first value (high threshold); a first power switch transistor (MP1, MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CK, CKB) to the first power switch transistor’s gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharging from the circuit arrangement; and a plurality of switching transistors (MP2, MN2), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater than the magnitude of the third value (high threshold voltage is larger than the low threshold voltage).

Applicants have amended claim 29 into independent form by incorporating all the limitations of claim 24 in claim 29. Applicants have amended all dependent claims to depend from claim 29 and canceled claim 24. Claim 29 has been found allowable (see paragraph 14 of the official action) and therefore claims 25-28, 30-37 and 39-50, as amended, are also allowable.

Applicants note that the term “each” in claim 29, line 13 has been replaced with “at least one.” Applicants respectfully state that this amendment does not adversely effect the allowability of the claim 29.

Additionally, Applicants have added new claim 51 incorporating all the limitations cancelled in claim 24 and pending claims 26 and 33. Applicants respectfully state that Claim 26 has been found allowable and therefore claim 51 is also allowable.

Claims 24-25, 27-28, 33-37, 45-46 and 49-50 stand rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,500,715 to Matsuzaki et al. (hereinafter "Matsuzaki").

Regarding these claims, the Examiner states that Matsuzaki discloses a circuit arrangement (See Figure 14) comprising a flip flop (LH1 details shown in figure 8) having a plurality of storage transistors with a threshold voltage of a first value (high threshold); a first power switch transistor (MN1) having a second threshold voltage (high threshold), wherein an application of a predetermined electrical potential (CS) to the first power switch transistor gate terminal brings the circuit arrangement to an operating state (standby mode) in which if at least one supply voltage is switched off, electric charge carriers (leakage current) contained in the circuit arrangement are prevented from discharging from the circuit arrangement; and a plurality of switching transistors (TP1-TP3, TN1-TN3), having a threshold voltage of a third value, provided between the flip flop and the first power switch transistor, for coupling the flip flop input signal (IN) into the flip flop, wherein the magnitude of the first and/or second value is greater than the magnitude of the third value (high threshold voltage is larger than the low threshold voltage).

Applicants have amended the claims to depend from claim 29 and rendered the above rejection to Matsuzaki moot.

Claims 39-42 stand rejected under 35 U.S.C. § 103(a) as being unpatentable for obviousness over Horiguchi or Matsuzaki in view of U.S. Patent No. 6,794,914 to Sani et al. (hereinafter "Sani").

Regarding claim 39-42, the Examiner states that Horiguchi or Matsuzaki disclose similar circuit arrangements however do not disclose a test circuit coupled to the flip flop for testing the functionality of the flip flop. The Examiner states that Sani teaches a flip flop having a test circuit to test and enhance the reliability of the flip flop. See Sani, figure 3 (reference no. 310). The Examiner states that it would have been obvious to one of ordinary skill in the art at the time the invention was made to include Sani's test circuit in the circuit arrangement of Horiguchi or Matsuzaki for the purpose of enhancing the reliability of the flip flop.

Applicants have amended the claims to depend from claim 29 and rendered the above rejection to over Horiguchi or Matsuzaki in view of Sani moot.

Claims 43-44 stand rejected under 35 U.S.C. § 103(a) as being unpatentable for obviousness over Matsuzaki in view of Sani.

Regarding claim 43-44, the Examiner states that Matsuzaki discloses a similar circuit arrangement however does not disclose test transistors coupled to the flip flop and having a gate thickness greater than the gate thickness of the transistors of the pulse generator. The Examiner states that Sani discloses a flip flop having a test circuit to test and enhance the reliability of the flip flop (see Sani, figure 3, ref. no. 310) and that it would have obvious to one of ordinary skill in the art at the time the invention was made to include Sani's test circuit in the circuit arrangement of Matsuzaki for the purpose of enhancing the reliability of the flip flop.

Applicants have amended the claims to depend from claim 29 and rendered the above rejection to over Matsuzaki in view of Sani moot.

CONCLUSION

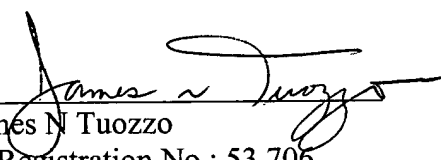
In view of the above amendments and remarks, it is believed that claims 25-37 and 39-51 are in condition for allowance and it is respectfully requested that the application be reconsidered and that all pending claims be allowed and the case passed to issue.

If there are any other issues remaining which the Examiner believes could be resolved through either, a Supplemental Response or an Examiner's Amendment, the Examiner is respectfully requested to contact the undersigned at the telephone number indicated below.

Dated: May 12, 2005

Respectfully submitted,

By


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Amendments to the Drawings

The replacement drawing sheets, which are presented in Attachment A, include changes to Figures 6 and 8. Specifically, changes were made to show transistor 602 as a pMOS field effect transistor as described in page 30, line 21 and claimed in claim 32. Additionally, Applicants have added figure 12 illustrating, in block diagram format, a common power switch transistor provided for the flip flop and for at least one additional flip flop. Support for FIG. 12 can be found in the specification page 10, lines 5-10 and page 24, lines 11-13.

Attachment A: Replacement Drawing Sheets